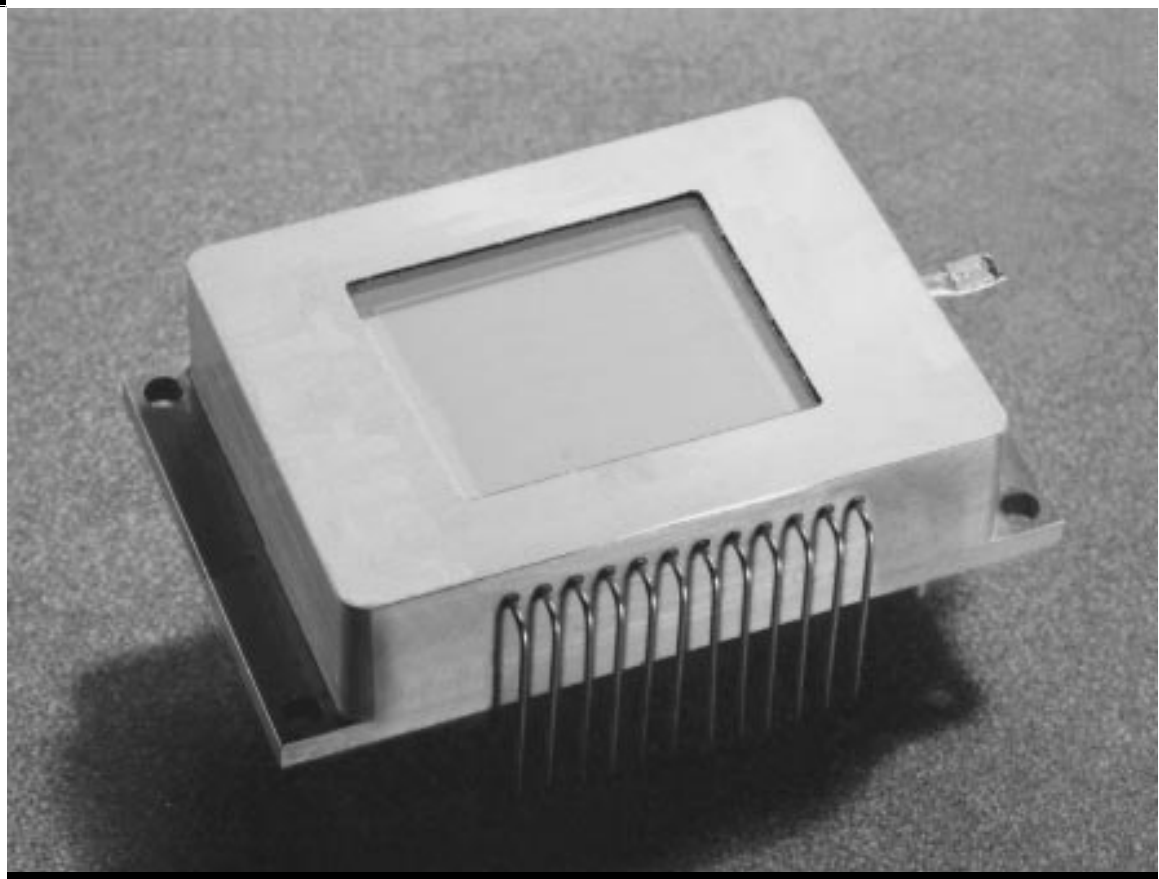

PRELIMINARY

SITe 1024 x 1024 Thermoelectrically Cooled Scientific-Grade CCD

SIA003A CCD Imager: *Ideal for applications with medium-area imaging and very low dark current requirements*

- 1024 x 1024 pixel format (24μm square)
- Front-illuminated or thinned, back-illuminated versions
- Packaged with a two stage Thermoelectric cooler for improved performance without a dewar
- Unique thinning and Quantum Efficiency enhancement processes
- Excellent QE from IR to UV
- Anti-reflection coating for visible region
- MPP technology
- Low dark current
- Excellent charge transfer efficiency (CTE) at all signal levels
- On-chip output MOSFET for low noise
- Wide dynamic range
- Applications include astronomy, machine vision, medical imaging, X-ray imaging, and scientific imaging

General Description

The SIA003A CCD Imager is a silicon charge-coupled device designed to efficiently image scenes at low light levels from UV to near infrared. The sensor is fabricated as a 1024 x 1024 pixel, full frame area imager that utilizes a buried channel, three level polysilicon gate process. Features include a buried channel with a mini-channel for high transfer efficiency, multi-phase pinned (MPP) operation for low dark current, and a lightly doped drain (LDD) amplifier for low read noise. The device is available in a front illuminated version or a thinned, back- illuminated version that provides superior quantum efficiency.

The CCD is thermoelectrically (TE) cooled using a two stage cooler that is an integral part of the package. The sealed vacuum package prevents the device from collecting moisture when it is cooled below dew point temperature and prevents thermal conduction of heat to the device. SITe's unique thinning and back surface enhancement process provides increased blue and UV response in a flat and fully supported die.

Thermoelectric Cooler

The two stage thermoelectric cooler mounted inside the sealed vacuum package can maintain the CCD at a temperature of approximately 65 to 70 degrees C lower than the external temperature of the heat sink. The external heat sink must be properly cooled for this to be accomplished. The dark current of the CCD is a strong function of temperature. It will double for about every 7ºC of temperature change. By maintaining the CCD at -35ºC, the dark current will be reduced to >200X less than its room temperature value. This is a significant reduction and worth the extra circuitry and cooling provisions needed to remove the heat from the heat sink. The thermoelectric cooler itself also generates heat during the cooling process so the heat being removed at the heat sink is greater than just the heat removed from the CCD.

Functional Description

Imaging Area

As shown in the functional diagram, Figure 2, the imaging area of the SIA003A consists of 1024 columns, each of which contains 1024 picture elements (pixels). Each pixel measures 24µm x 24µm. The columns are isolated from each other by channel-stop regions. There is an output amplifier at each corner of the device, at each end of the two output serial registers. By proper phasing of the parallel and serial clocks any of the four amplifiers may be selected, but only one may be operated at a time.

The signal charge collected in the imaging array is transferred along the columns, one row at a time, to one of the serial registers and from there to the desired output amplifier

Three levels of polysilicon are used to fabricate the three gate electrodes which form the basic CCD cell (pixel). All of the pixels in a given row are defined by the same three gates. Corresponding gates in each row within a group of 1024 are connected in parallel at both edges of the array. The clock signals used to drive the imaging area gates are brought in from both edges of the array, thus increasing the rate at which the rows can be shifted.

Serial Registers

The functional diagram (Figure 2) illustrates the relationship between the imaging array and the serial registers. The charge collected in the imaging section is transferred through the transfer gate into the serial register phase 1 gate. The serial register has one pixel for each column in the imaging array, plus 16 extra pixels at each end for a total of 1056. The extra pixels serve as dark reference and ensure that the signal chain is stabilized when the image data is received at the output.

The output of both serial registers is terminated in a summing well, a DC-biased last gate (which serves to decouple the serial clock pulses from the output node), and an output amplifier. The summing well is a separately clocked gate equal in charge capacity to the other serial gates. It can function to provide on-chip (noiseless) charge summing of consecutive serial pixels. Similarly, it is possible to sum pixels into the serial register by performing repetitive parallel transfers with the serial clocks fixed. In this manner, it is possible to collect and detect as one pixel the sum of the charge in sub-arrays of the imaging section, provided that the sum is less than the full well charge. The well capacity of a pixel in the serial register is greater than that of a parallel pixel to ensure that the CTE remains high.

This architecture permits images to be read out of any one of the four output amplifiers, but only one at a time.

Output Structure

The imager has four output MOSFETs that are located in each corner of the device at the ends of the extended serial registers. Figure 1 presents a schematic diagram of each output configuration. For the SIA003A product, all the four output amplifier reset gates (RG), reset drains (RD), summing wells (SW), and last gates (LG) are internally connected in parallel and individually brought out to a single pin. This reduces the pin count and the conductive heat load from the package to the cooled CCD through the bond wires.

In operation, a positive pulse is applied to the reset gate (RG). This sets the potential of the floating diffusion to the potential applied to the reset transistor drain (RD). The reset gate voltage is then turned off and the output node (the floating diffusion) is isolated from the rest of the circuit. Charge from the serial pixel is then transferred to the output node on the falling edge of the summing well (SW) clock signal. The addition of charge on the output node causes a change in the voltage on the gate of the output MOSFET. This change in voltage is sensed at OUTx.

Timing

The SITe SIA003A CCD Imager can only be operated with one output operating at a time, but all four outputs have the appropriate pinouts and can be individually

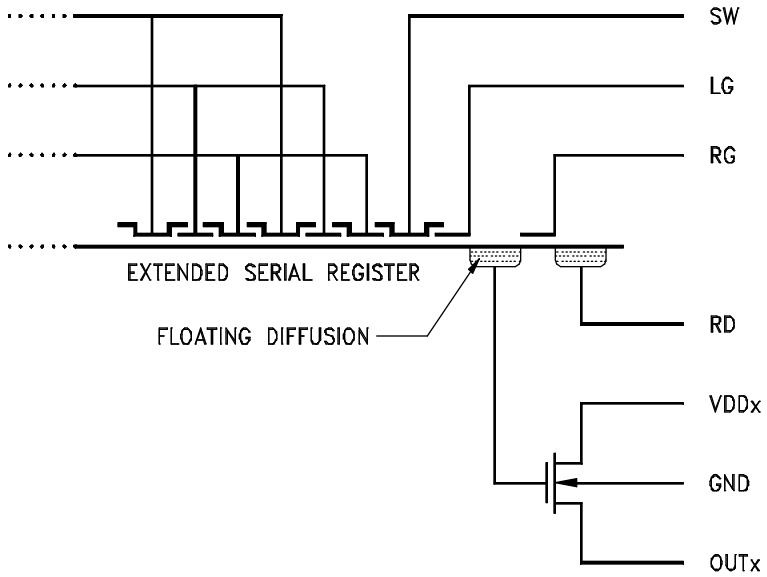

FIGURE 1 *Output Structure*

selected through proper clocking. The serial and parallel gates are not separated into quadrants as with the SI-003A. Both serial gates are internally connected and clocked together. The parallel gates are also internally connected within the package and driven together. This arrangement saves many pins and also reduces the heat load on the CCD by conduction through the bond wires to the package.

The device operates in the full frame mode where the entire imager's signal is transferred to one of the selected outputs. This timing is shown in Figure 4, The same numbered phases of both of the serial registers are internally connected and clocked together. Likewise, all the same numbered phases of the parallel registers are internally connected and clocked together.

The signal charge may be clocked out of any of the four outputs but the timing must be appropriate for the selected output. The transfer gate (TG) adjacent to the selected serial register must be clocked. The other transfer gate should be held low to prevent unwanted charge in the unused serial register from entering the parallel register. The unused serial register's gates will clocked since all the phases of both serial registers are internally connected. Both upper and lower transfer gates (TGU and TGL) are available at package pins for clocking or to apply a bias voltage.

Timing diagrams for each output are shown in Figure 3. During a parallel or serial shift, the signal charge is transferred one pixel at a time. A frame readout consists of at least 1024 parallel shift and serial readout sequences for a full frame. Figure 4 shows the typical timing for a full frame readout. A serial readout sequence consists of at least 1056 serial shifts for full frame mode (16 for each serial extended region plus 1024 pixels of data from the imaging array). The serials are static when the parallels are shifting and vice-versa. During integration, the serial clocks are normally kept running continuously to flush the serial registers and to stabilize the bias levels in the off-chip signal chain.

The timing diagrams (Figures 3 and 4) are for integration under phases 1 and 2. For MPP operation, this timing is a requirement (as it is with all SITe MPP devices). For non-MPP operation this is a desirable option, since the number of rows will remain the same as for MPP operation. For reference, typical timing for the clamp and sample signal of an external charge detection circuit are included in the output timing diagrams.

Multi-Phase Pinned (MPP) Operation

The multi-phase pinned (MPP) technology used on the SIA003A allows the device to be operated totally inverted during integration and line readout. The main advantage of this mode of operation is that it results in much lower dark current than conventional CCD operation. Other advantages of MPP operation are the reduction of surface residual image effects and a greater tolerance for ionizing radiation environments.

To operate the CCD in the MPP mode, the array clocks are biased sufficiently negative to invert the n-buried channel and "pin" the surface potential beneath each phase to the substrate potential. This allows holes from the p+ channel stop to populate the surface states at the silicon/silicon dioxide interface, minimizing surface dark current generation.

To enable all three phases of the array to be inverted and still retain well capacity, MPP devices have an extra implant under the phase 3 gates. During integration, this creates a potential barrier between each pixel allowing signal charge to accumulate under phases 1 and 2 at each pixel site. A consequence of this mode of operation is that the total well capacity is about 50 percent of that of a standard CCD if all the parallel clocks are operated at the same voltages. A larger well capacity can be obtained if phase 3 parallel clock high rail is operated about 3 volts higher than the phase 1 and phase 2 high rails.

DEVICE SPECIFICATIONS

Measured at -45 deg. C, unless otherwise indicated, 45 kpixels/sec and standard voltages using a dual slope CDS circuit (8 µs integration time)

	Minimum	*Typical*	*Maximum*
Format		1024 x 1024 pixels	
Pixel Size		24 µm x 24 µm	
Imaging Area		24.6 mm x 24.6 mm	
Dark current (MPP), *20° C equivalent*		50 pa/cm^2	70 pa/cm^2
Readout noise Front		5 electrons	9 electrons
Back		7 electrons	10 electrons
Full Well signal	300,000 electrons	350,000 electrons	
Output gain	1.0 µV/ electron	1.5 µV/ electron	
CTE per pixel	0.99995	0.99999	
Storage Temperature	-20		+60
Temperature Sensor		Analog Devices, AD590	

TE COOLER SPECIFICATIONS

(Assumes 5mW of optical energy on the CCD array.)

Parameter	*Minimum*	*Typical*	*Maximum*
Heat Sink Power Load (watts)		19	26
Voltage (volts)		12	
Current (amps)		1.5	2
CCD Temperature (°C)	-45	-35	
Heat Sink Temperature (°C)		35	

TABLE 1 *Device specifications, SIA003A*

DC OPERATING CONDITIONS

TERMINAL	ITEM	MIN	STANDARD	MAX	UNIT
VDDx	OUTPUT DRAIN SUPPLY	22	24	26	V
RDx	RESET DRAIN	13	15	17	V
LGx	LAST GATE	-4	-2	0	V
SUB,PKG	SUB & PACKAGE CONNECTION		0		V
GNDx	MOSFET GROUND REFERENCE		0		V
OUTx	MOSFET OUTPUT (LOAD)	5	20	50	kohms

GATE TO SUBSTRATE VOLTAGES

TERMINAL	ITEM		MIN	STANDARD	MAX	P TO P MAX	UNIT
RGx	RESET GATE	LOW RAIL	-5	0	5	20	V
		HIGH RAIL	5	12	15		V
S#x	SERIAL GATE	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V
SWx	SUMMING WELL	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V
P#x	PARALLEL GATE	LOW RAIL	-10	-9	0	20	V
		HIGH RAIL	0	4	10		V
P3		HIGH RAIL	0	7	10		V
TGx	TRANSFER GATE	LOW RAIL	-10	-9	0	20	V
		HIGH RAIL	0	7	10		V

TABLE 2 *DC operating conditions and clock voltages,* SIA003A

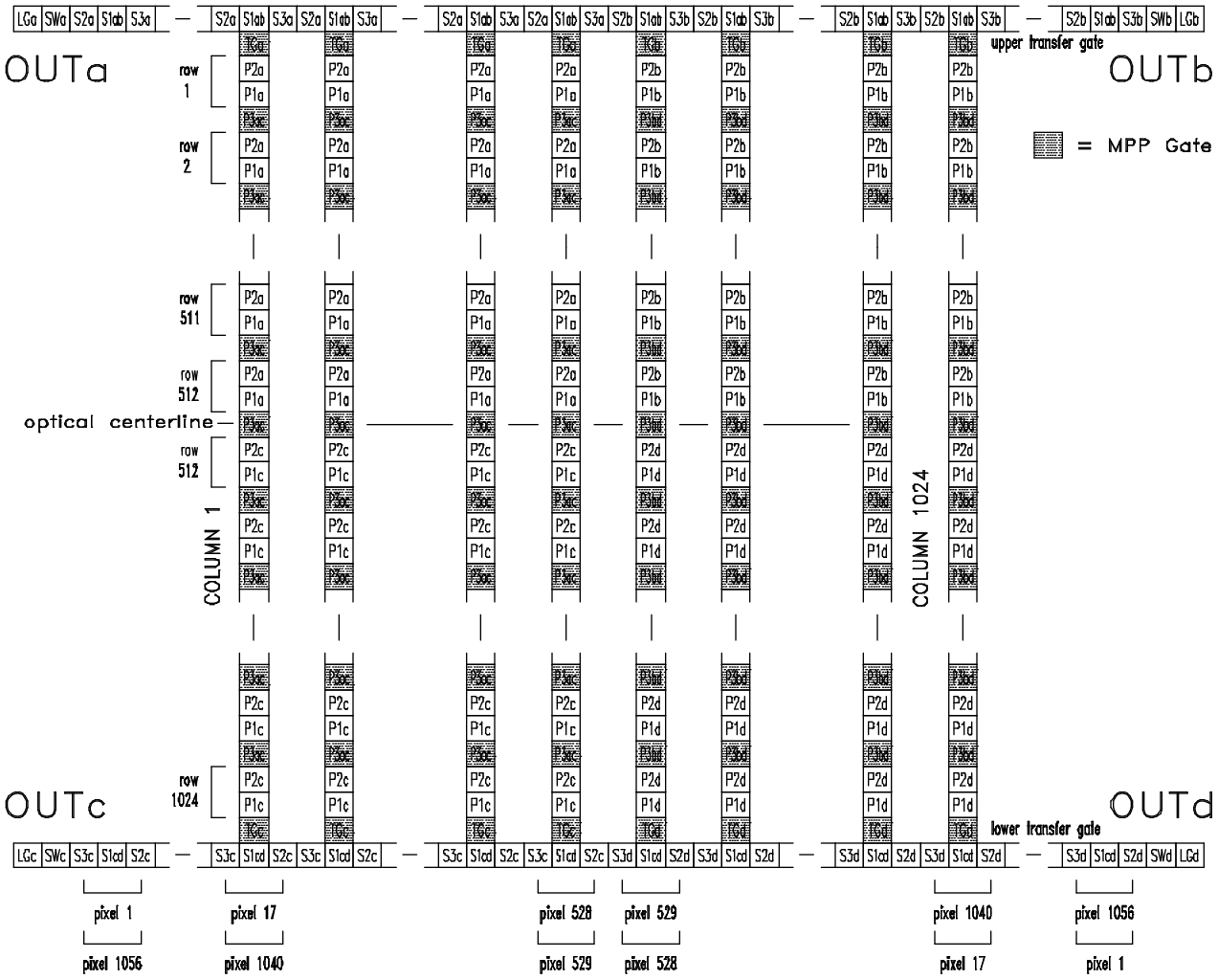

FIGURE 2 SIA003A *functional diagram*

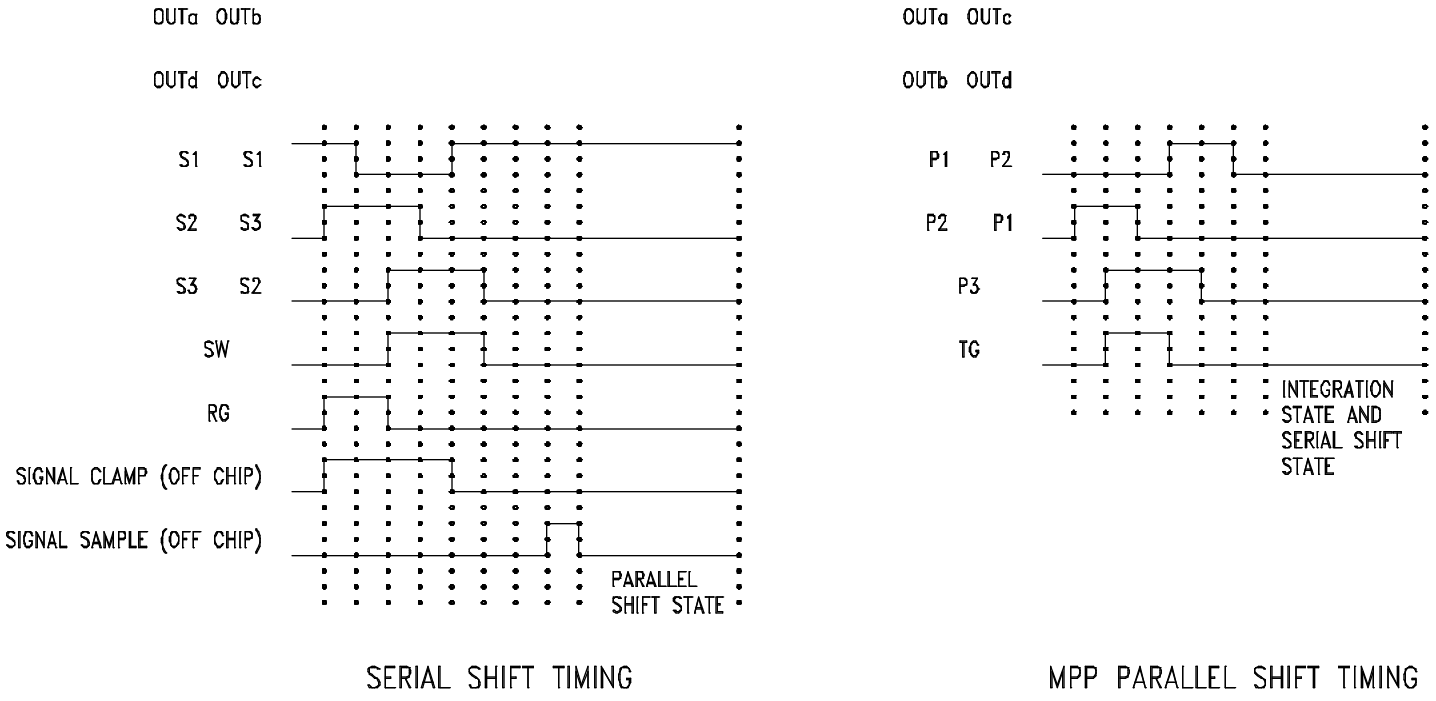

FIGURE 3 *Serial and Parallel timing for all outputs*

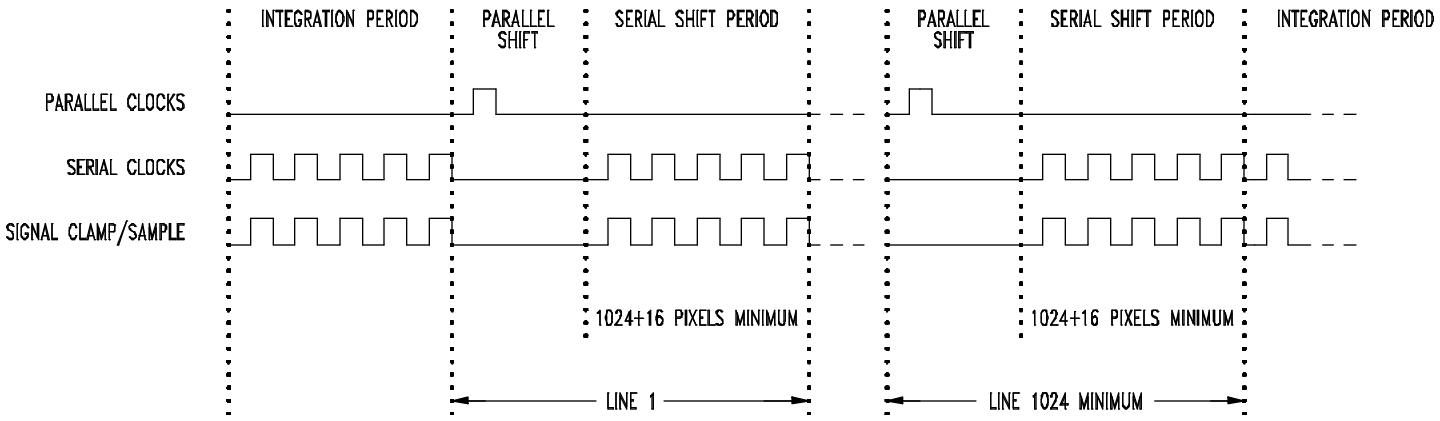

FIGURE 4 *Typical full-frame readout*

SIA003A PIN DEFINITION

PIN #	FUNCTION	REGISTERS	SYMBOL
1	Output transistor drain, c output	c register	VDDc
2	Output transistor source, c output	c register	OUTc
3	Substrate Ground		SUB
4	Transfer gate, lower serial register	cd register	TGL
5	Parallel phase 1	all registers	P1
6	Last gate, all outputs	both serial registers	LG
7	Parallel phase 2	all registers	P2
8	Parallel phase 3	all registers	P3
9	Transfer gate, upper serial register	ab register	TGU
10	Chip Ground		GND
11	Output transistor source, d output	cd register	OUTd
12	Output transistor drain, d output	cd register	VDDd
13	Output transistor drain, b output	ab register	VDDb
14	Output transistor source, b output	ab register	OUTb
15	Summing well, all outputs	both serial registers	SW
16	Reset transistor gate, all outputs	both serial registers	RG
17	Serial phase 1	both serial registers	S1
18	Temperature Sensor Diode - Negative		TSD (-)
19	Temperature Sensor Diode - Positive		TSD (+)
20	Serial phase 2	both serial registers	S2
21	Serial phase 3	both serial registers	S3
22	Reset Gate, all outputs	both serial registers	RG
23	Output transistor source, a output	ab register	OUTa
24	Output transistor drain, a output	ab register	VDDa
BOTTOM	TEC POWER SUPPLY		TEC(+)
BOTTOM	TEC POWER SUPPLY		TEC(-)

TABLE 3 *pin definitions*

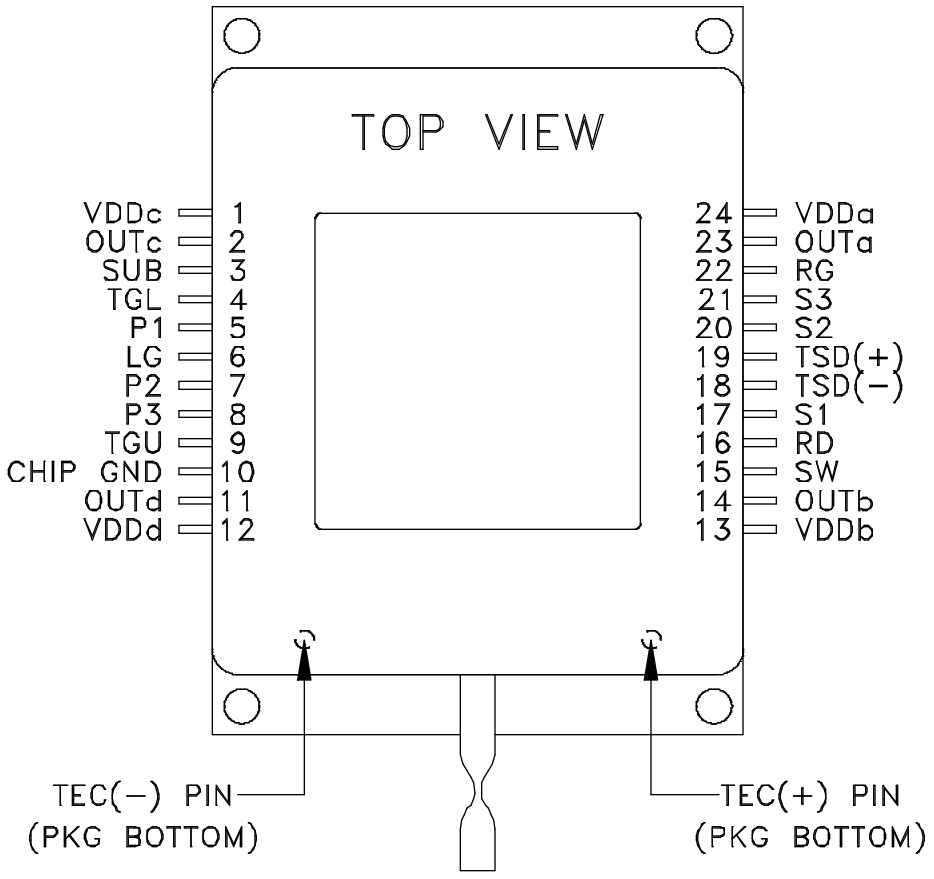

FIGURE 5 SIA003A *pin labels*

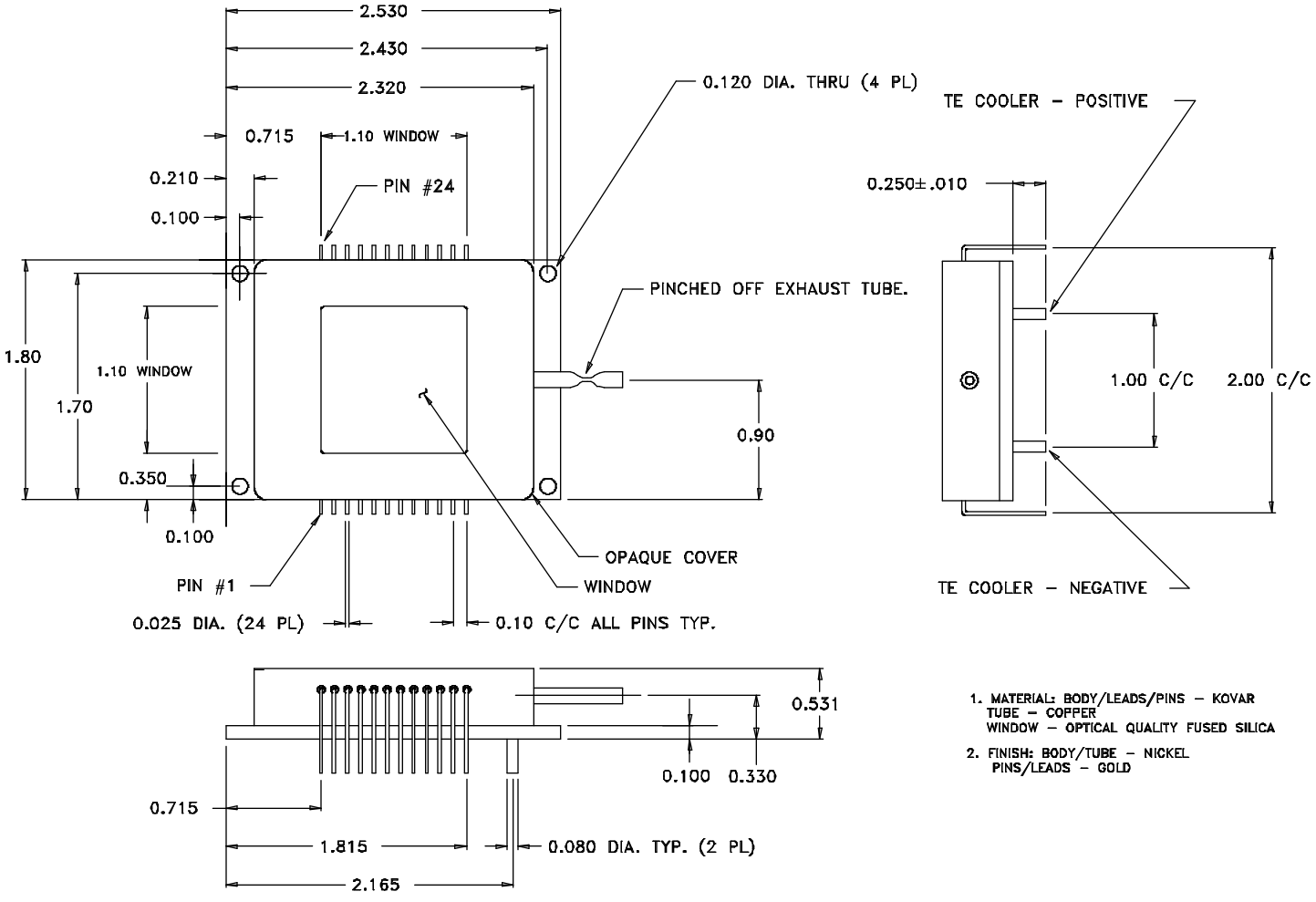

FIGURE 6 SIA003A *package configuration*

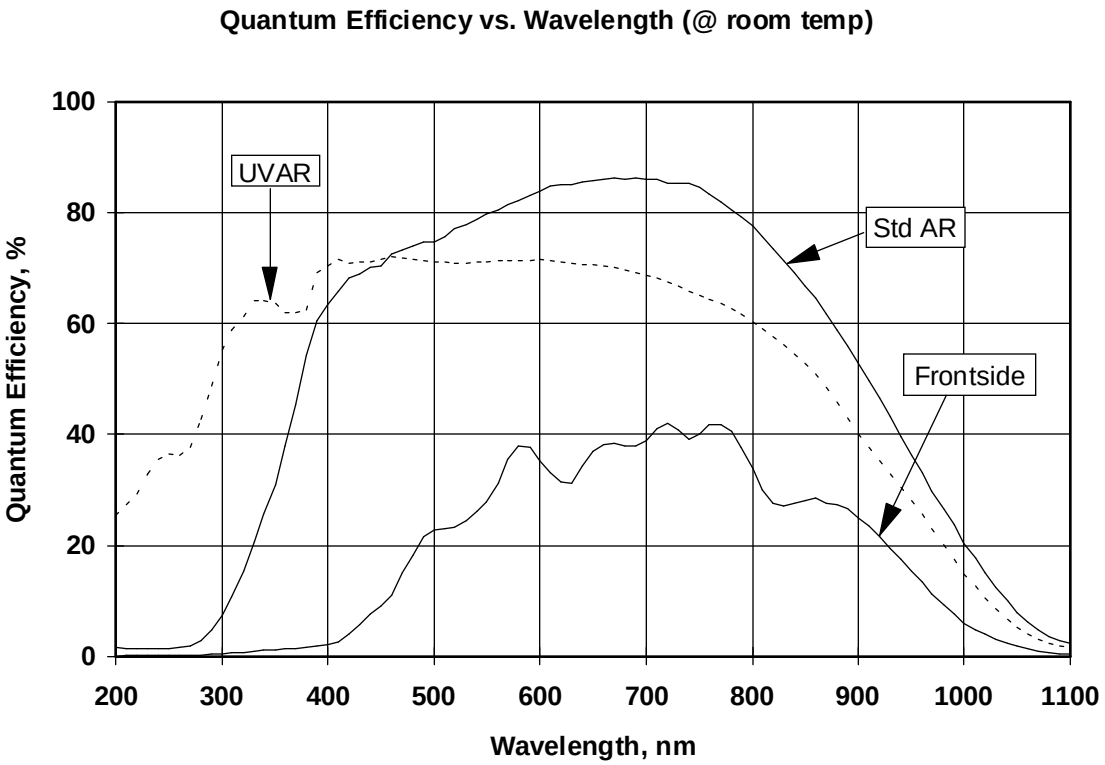

FIGURE 7 *Typical QE curves*

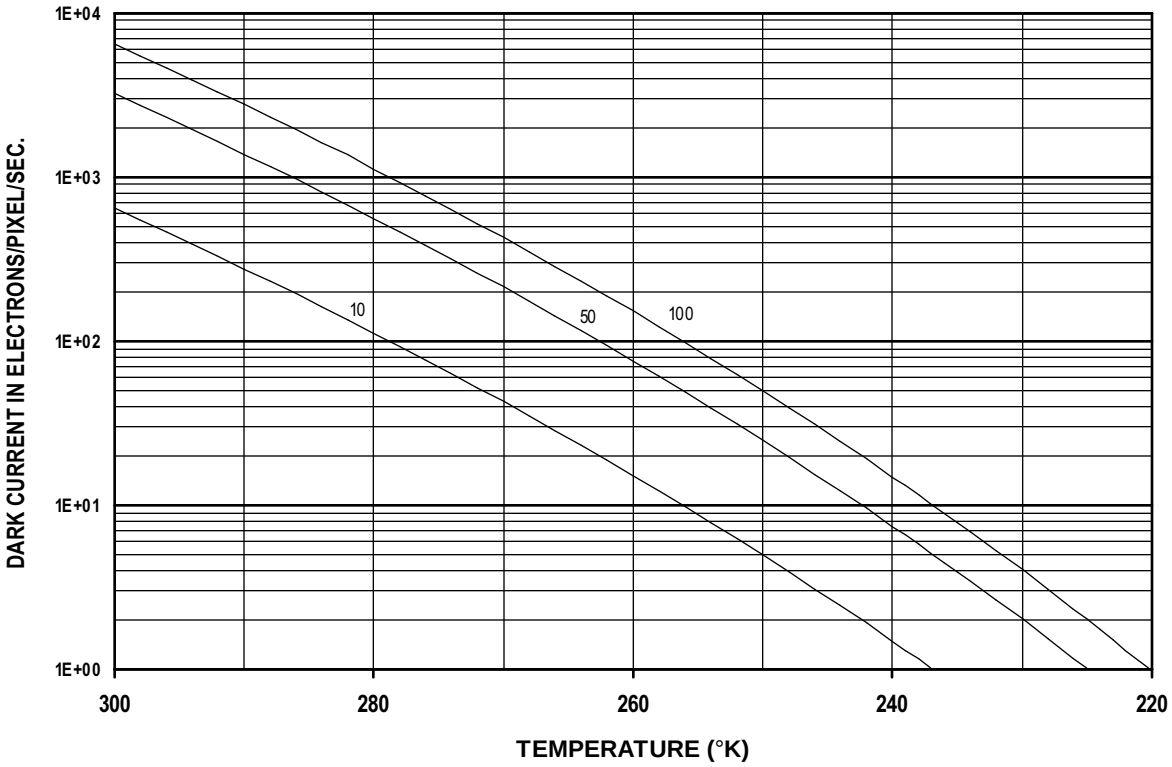

FIGURE 8 *Effect of temperature on dark current. Parameter is pAmp/cm^2 at 293K*

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Scientific Imaging Technologies, Inc. (SITe) specializes in the research, design, and manufacture of charge-coupled devices (CCDs) and imaging subassemblies containing CCD components. SITe's scientific grade CCDs are used in applications for astronomy, aerospace, medical, military surveillance, spectroscopy, and other areas of imaging research. Commercial uses of SITe high performance CCDs include such areas as biomedical imaging, manufacturing quality control, environmental monitoring, and nondestructive testing.

With its focus on scientific-grade CCD imaging components and modules, SITe provides standard designs, user defined custom CCDs, and foundry services. SITe's engineering and manufacturing team builds custom CCD imagers for use in the most demanding applications including NASA programs, satellite platforms, and other research projects. Device formats are available as front illuminated or thinned, back illuminated CCDs.

Innovation, process development, and design experience date back to the founding of the group in 1974.

SITe Lit. No. SIA003A
revision date: 12/21/95

Product Precautions

Scientific Imaging Technologies, Inc. (SITe) realizes the use of charge-coupled devices (CCDs) for imaging is rapidly expanding into new applications. Awareness of the sensitivity of CCDs to electrostatic discharge (ESD) damage and the steps that can be implemented to prevent damage are very important to the end user.

With the exception of the back-illuminated SI424A, SITe imagers do not have built-in gate protection structures. Even with the protection structures, the imagers are very sensitive to ESD damage. It is imperative that proper precautions be taken whenever the imagers are handled.

The damage caused by ESD can be immediate and fatal (hard damage) resulting in a completely nonfunctional device. ESD damage can also be more subtle with no immediate device performance degradation. In this case, the result is a slow deterioration (soft damage) that may not be apparent until after extended operation.

There are three major areas where special procedures are required. We recommend that our customers use these procedures to minimize the risk of ESD damage.

1. Work areas specifically designed to minimize ESD.

2. Personnel requirements for ESD damage protection.

3. Use special ESD protected handling and shipping containers. SITe has developed a custom shipping container which grounds all the CCD pins together and allows clean and safe handling for incoming inspection and storage.

For more specific information on minimizing ESD damage, refer to SITe's technical briefing called "Recommended ESD Handling Procedures For CCD Imagers."