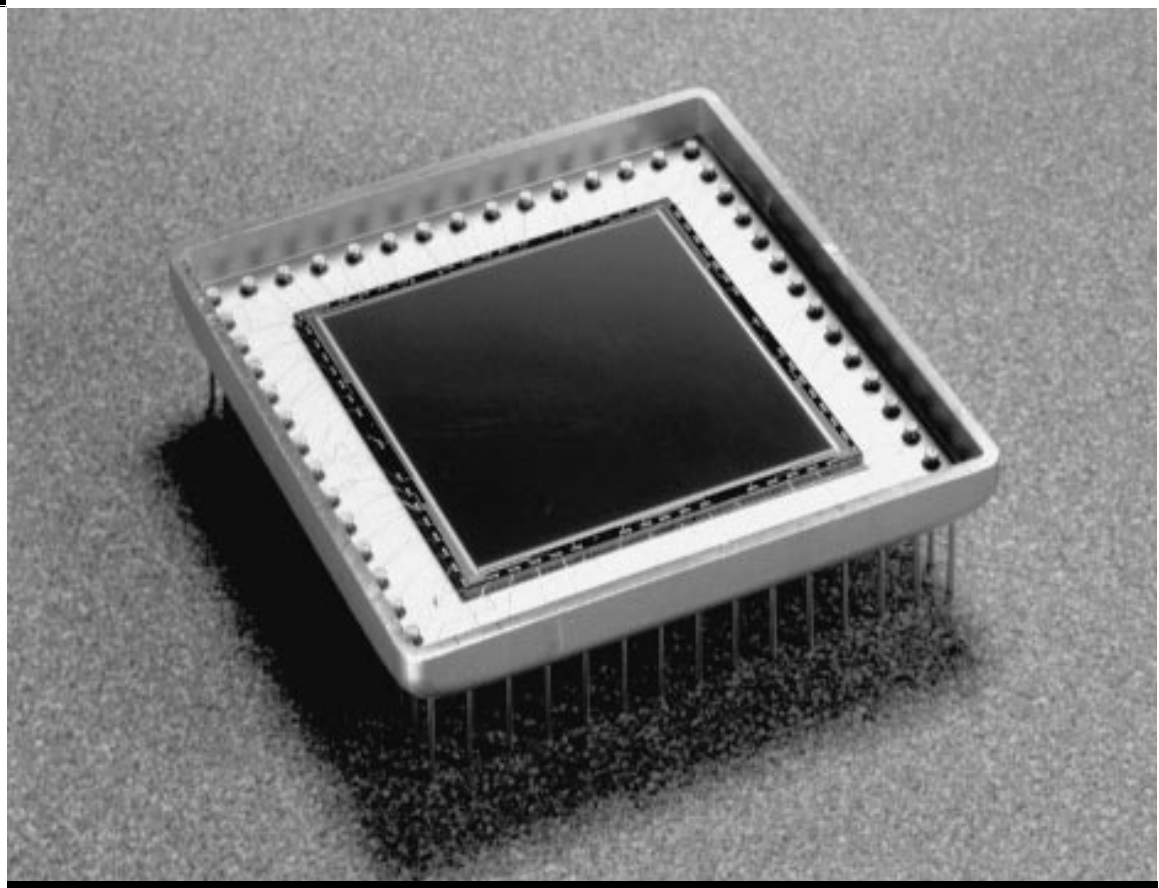

PRELIMINARY

SITe 1024 x 1024 Scientific-Grade CCD

SI-003A CCD Imager: *Ideal for applications with medium-area imaging requirements*

- 1024 x 1024 pixel format (24μm square)
- Front-illuminated or thinned, back-illuminated versions
- Unique thinning and Quantum Efficiency enhancement processes
- Excellent QE from IR to UV
- Anti-reflection coating for visible region
- Mechanical Rigidity
- MPP technology
- Low dark current
- Excellent charge transfer efficiency (CTE) at all signal levels
- On-chip output MOSFET for low noise
- Wide dynamic range
- Serial-parallel-serial architecture with output MOSFETs in each quadrant for maximized readout flexibility
- Applications include astronomy, machine vision, medical imaging, X-ray imaging, and scientific imaging

General Description

The SI-003A CCD Imager is a silicon charge-coupled device designed to efficiently image scenes at low light levels from UV to near infrared. The sensor is fabricated as a 1024 x 1024 pixel, full frame area imager that utilizes a buried channel, three level polysilicon gate process. Features include a buried channel with a mini-channel for high transfer efficiency, multi-phase pinned (MPP) operation for low dark current, and lightly doped drain (LDD) output amplifiers for low read noise. The device is available in a front illuminated version or a thinned, back-illuminated version that provides superior quantum efficiency.

SITe's unique thinning and back surface enhancement process provides increased blue and UV response in a flat and fully supported die. The CCD imager is mounted in a non-hermetic metal package without a window.

Functional Description

Imaging Area

As shown in the functional diagram, Figure 2, the imaging area of the SI-003A consists of 1024 columns, each of which contains 1024 picture elements (pixels). Each pixel measures 24µm x 24µm. The columns are isolated from each other by channel-stop regions. The 1024 rows of pixels are further divided into two groups of 512 rows (upper section) and 512 rows (lower section) for clocking flexibility and output amplifier selection. There is an output amplifier at each corner of the device, at each end of the two output serial registers. By proper phasing of the parallel and serial clocks any or all of the four amplifiers may be selected.

The signal charge collected in the imaging array is transferred along the columns, one row at a time, to one or both of the serial registers and from there to the desired output amplifiers. The serial registers are also divided into two sections. Thus the array can be divided into quadrants to maximize data transfer. The four quadrants are designated by the letters a,b,c,d, corresponding to the nearest amplifier.

Three levels of polysilicon are used to fabricate the three gate electrodes which form the basic CCD cell (pixel). All of the pixels in a given row are defined by the same three gates. Corresponding gates in each row within a group of 512 are connected in parallel at both edges of the array. The clock signals used to drive the imaging area gates are brought in from both edges of the array, thus increasing the rate at which the rows can be shifted. The two sections of the imaging area are bussed independently for phases 1 and 2, but the phase 3 bus is common to both sections.

Serial Registers

The functional diagram (Figure 2) illustrates the relationship between the imaging array and the serial registers. The charge collected in the imaging section is transferred through the transfer gate into the serial register phase 1 gate. The serial register has one pixel for each column in the imaging array, plus 16 extra pixels at each end for a total of 1056. The extra pixels serve as dark reference and ensure that the signal chain is stabilized when the image data is received at the output.

as in Figure 4, the entire imager's signal is transferred to one output, and all of the same

The output of both serial registers is terminated in a summing well, a DC-biased last gate (which serves to decouple the serial clock pulses from the output node), and an output amplifier. The summing well is a separately clocked gate equal in charge capacity to the other serial gates. It can be used to provide on-chip (noiseless) charge summing of consecutive serial pixels. Similarly, it is possible to sum pixels into the serial register by performing repetitive parallel transfers with the serial clocks fixed. In this manner, it is possible to collect and detect as one pixel the sum of the charge in sub-arrays of the imaging section, provided that the sum is less than the full well charge. The well capacity of a pixel in the serial register is greater than that of a parallel pixel to ensure that the CTE remains high.

The two sections of the serial registers are bussed separately for phases 1 and 2, but the phase 1 bus is common to both sections within each serial register. As a result, S1ab and S1cd are driven by a common phase 1 clock for each specific register.

This architecture permits images to be read out of any one or all of the four output amplifiers in a variety of ways. Four major options are represented in the CCD timing diagrams and are described in a later section.

Output Structure

The imager has four output MOSFETs that are located in each corner of the device at the ends of the extended serial registers. Figure 1 presents a schematic diagram of each output configuration.

In operation, a positive pulse is applied to the reset gate (RGx). This sets the potential of the floating diffusion to the potential applied to the reset transistor drain (RDx). The reset gate voltage is then turned off and the output node (the floating diffusion) is isolated from the rest of the circuit. Charge from the serial pixel is then transferred to the output node on the falling edge of the summing well (SWx) clock signal. The addition of charge on the output node causes a change in the voltage on the gate of the output MOSFET. This change in voltage is sensed at OUTx.

Timing

The SITe SI-003A CCD Imager can be operated with one, two, three or four outputs operating simultaneously. The serial gates are separated into left and right halves. Similarly, the parallel gates are separated into upper and lower halves. The quadrants thus formed are designated a (upper left), b (upper right), c (lower left), and d (lower right). See Figure 2.

When operated in the full frame mode,

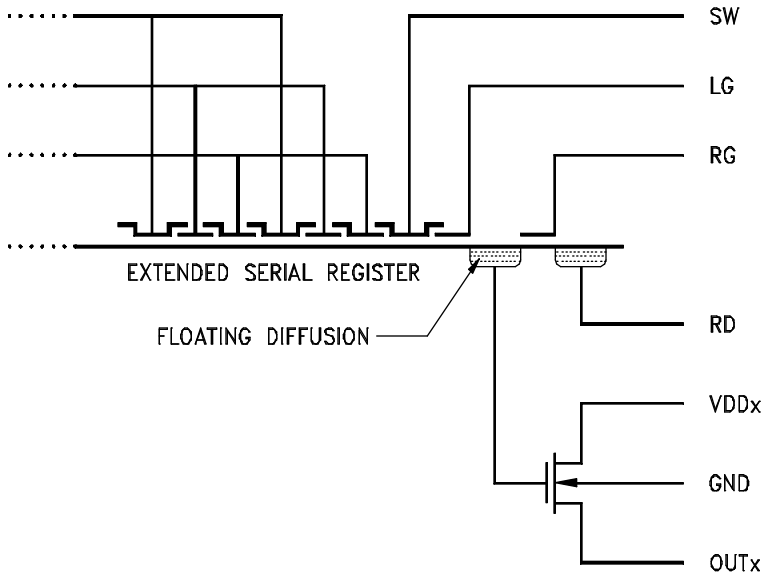

FIGURE 1 *Output Structure*

numbered phases of the selected serial register are clocked together. For example, S2a and S2b would be wired together. Likewise, in the parallel registers, P1a, P1b, P1c and P1d would all be wired and clocked together. The signal charge may be clocked out of any output; however, the timing must be appropriate for that output. The transfer gate (TG) adjacent to the chosen serial register must be clocked. The other transfer gate should be held low to prevent unwanted charge in the unused serial register from entering the parallel register. The unused serial register's gates could be either clocked or held at the proper dc level.

The SI-003A may also be operated in the quad mode wherein the signal charge is clocked out of all four outputs simultaneously. The charge in each quadrant is transferred to the nearest output. The gates in each quadrant are given clocking signals appropriate for full frame operation of that output. For example, S1ab, S2a, S3a and SWa would be clocked according to A out timing, and S1ab, S2b, S3b and SWb would be clocked according to B out timing. Likewise, the parallels, P1a, P1b, P2a, P2b, P3a, P3b, TGa and TGb should all be clocked according to A out / B out parallel timing, and the lower half parallel and serial clocks would be clocked according to C out / D out timing.

Finally, the SI-003A may be operated with two simultaneous outputs by splitting either the serial or the parallel clocks. Timing for each of the halves must be appropriate for the chosen outputs. For example, to operate the split serials using outputs A and B; S1ab, S2a, S3a and SWa would be clocked according to A out serial timing while S1ab, S2b, S3b, and SWb would be clocked according to B out serial timing. The parallels would be operated as for full-frame using either A out or B out. To operate with a parallel split, the parallels would be operated in the quad split mode, while the serials would be clocked in the full-frame mode.

Timing diagrams for each output are shown in Figure 3. During a parallel or serial shift, the signal charge is transferred one pixel at a time. A frame readout consists of at least 1024 parallel shift/serial readout sequences for full frame; 512 for split parallels. Figure 4 shows the typical timing for a full frame readout. A serial readout sequence consists of at least 1056 serial shifts for full frame mode (16 for each serial extended region plus 1024 pixels of data from the imaging array); 528 (512+16) for split serial modes. The serials are static when the parallels are shifting and vice-versa. During integration, the serial clocks are normally kept running continuously to flush the serial registers and to stabilize the bias levels in the off-chip signal chain.

The timing diagrams (Figures 3 and 4) are for integration under phases 1 and 2. For MPP operation, this timing is a requirement (as it is with all SITe MPP devices). For non-MPP operation this is a desirable option, since the number of rows will remain the same as for MPP operation. For reference, typical timing for the clamp and sample signal of an external charge detection circuit are included in the output timing diagrams.

Multi-Phase Pinned (MPP) Operation

The multi-phase pinned (MPP) technology used on the SI-003A allows the device to be operated totally inverted during integration and line readout. The main advantage of this mode of operation is that it results in much lower dark current than conventional CCD operation. Other advantages of MPP operation are the reduction of surface residual image defect and a greater tolerance for ionizing radiation environments.

To operate the CCD in the MPP mode, the array clocks are biased sufficiently negative to invert the n-buried channel and "pin" the surface potential beneath each phase to the substrate potential. This allows holes from the p+ channel stop to populate the surface states at the silicon/silicon dioxide interface, minimizing surface dark current generation.

To enable all three phases of the array to be inverted and still retain well capacity, MPP devices have an extra implant under the phase 3 gates. During integration, this creates a potential barrier between each pixel allowing signal charge to accumulate under phases 1 and 2 at each pixel site. A consequence of this mode of operation is that the total well capacity is about 50 percent of that of a standard CCD if all the parallel clocks are operated at the same voltages. A larger well capacity can be obtained if phase 3 parallel clock high rail is operated about 3 volts higher than the phase 1 and phase 2 high rails.

DEVICE SPECIFICATIONS

Measured at -45 deg. C, unless otherwise indicated, 45 kpixels/sec and standard voltages using a dual slope CDS circuit (8 µs integration time)

		Minimum	*Typical*	*Maximum*
Format			1024 x 1024 pixels	
Pixel Size			24 µm x 24 µm	
Imaging Area			24.6 mm x 24.6 mm	
Dark current (MPP), *20° C equivalent*			50 pa/cm^2	70 pa/cm^2
Readout noise	Front		5 electrons	9 electrons
	Back		7 electrons	10 electrons
Full Well signal		300,000 electrons	350,000 electrons	
Output gain		1.0 µV/ electron	1.5 µV/ electron	
CTE per pixel		0.99995	0.99999	

TABLE 1 *Device specifications, SI-003A*

DC OPERATING CONDITIONS

TERMINAL	ITEM	MIN	STANDARD	MAX	UNIT
VDDx	OUTPUT DRAIN SUPPLY	22	24	26	V
RDx	RESET DRAIN	13	15	17	V
LGx	LAST GATE	-4	-2	0	V
SUB,PKG	SUB & PACKAGE CONNECTION		0		V
GNDx	MOSFET GROUND REFERENCE		0		V
OUTx	MOSFET OUTPUT (LOAD)	5	20	50	kohms

GATE TO SUBSTRATE VOLTAGES

TERMINAL	ITEM		MIN	STANDARD	MAX	P TO P MAX	UNIT
RGx	RESET GATE	LOW RAIL	-5	0	5	20	V
		HIGH RAIL	5	12	15		V
S#x	SERIAL GATE	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V
SWx	SUMMING WELL	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V
P#x	PARALLEL GATE	LOW RAIL	-10	-9	0	20	V
		HIGH RAIL	0	4	10		V
P3		HIGH RAIL	0	7	10		V
TGx	TRANSFER GATE	LOW RAIL	-10	-9	0	20	V
		HIGH RAIL	0	7	10		V

TABLE 2 *DC operating conditions and clock voltages,* SI-003A

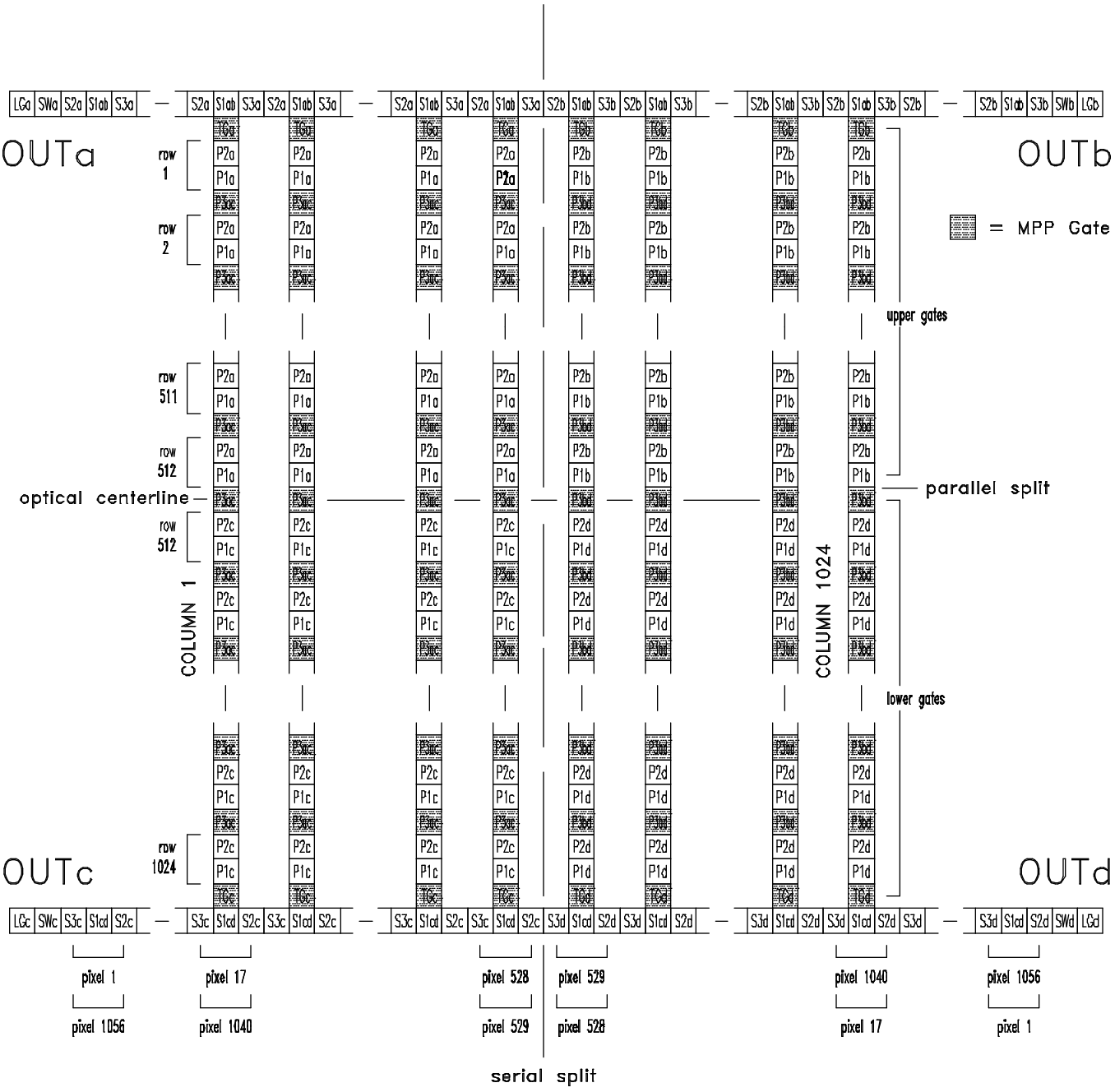

FIGURE 2 SI-003A *functional diagram*

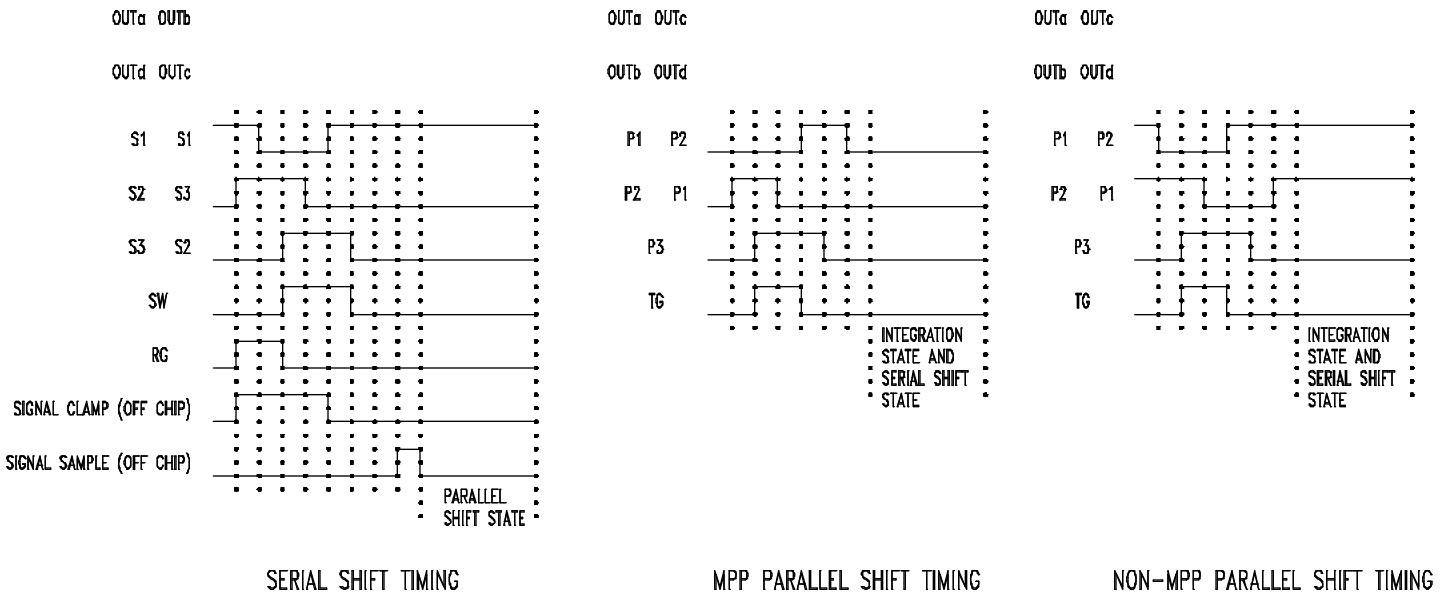

FIGURE 3 *Serial and Parallel timing for all outputs*

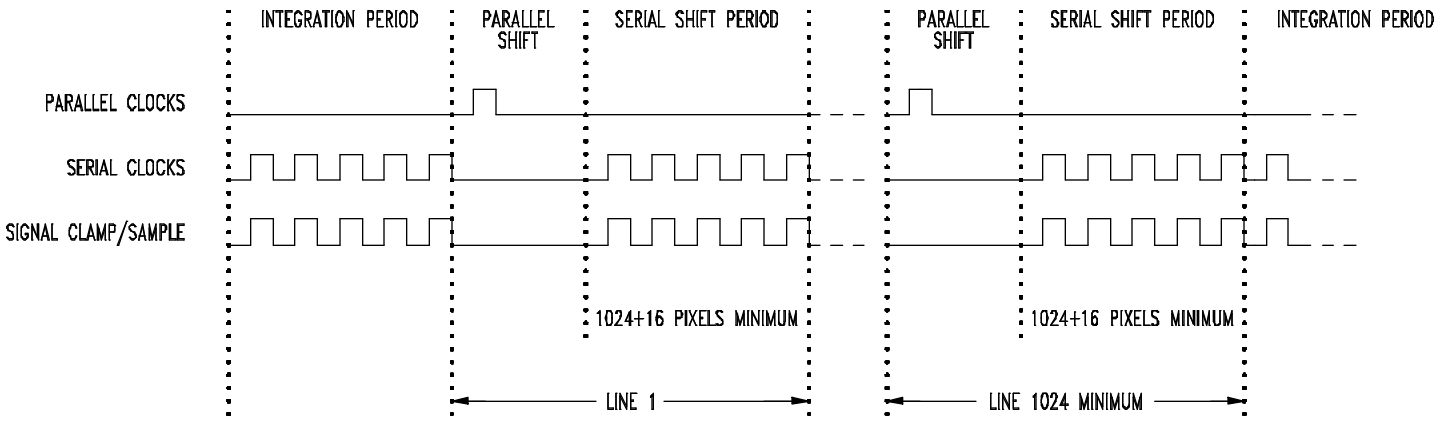

FIGURE 4 *Typical full-frame readout*

SI-003A PIN DEFINITION			
PIN # (BACK)	**FUNCTION**	**REGISTERS**	**SYMBOL**
1	Output transistor source, c output	c register	OUTc
2	Substrate and Package Ground		SUB
3	Reset Drain Supply, c output	c register	RDc
4	Reset Gate, c output	c register	RGc
5	Last gate, c output	c register	LGc
6 (7)	Serial phase 3, c register	c register	S3c
7 (6)	Serial phase 2, c register	c register	S2c
8	Serial phase 1, common cd register	cd register	S1cd
9 (10)	Serial phase 2, d register	d register	S2d
10 (9)	Serial phase 3, d register	d register	S3d
11	Last gate, d output	d register	LGd
12	Reset transistor gate, d output	d register	RGd
13	Reset transistor drain, d output	d register	RDd
14	Substrate and Package Ground		SUB
15	Output transistor source, d output	d register	OUTd
16	Output transistor drain, d output	d register	VDDd
17	Output Ground Reference	d register	GNDd
18	Summing well, d output	d register	SWd
19	Transfer gate, lower serial register	cd register	TGd
20	Parallel phase 1	lower quadrants	P1d
21	Parallel phase 2	lower quadrants	P2d
22	Parallel phase 3	right common	P3bd
23	Parallel phase 2	upper quadrants	P2b
24	Parallel phase 1	upper quadrants	P1b
25	Transfer gate, upper serial register	ab register	TGb
26	Summing well, b output	b register	SWb
27	Output Ground Reference	b register	GNDb
28	Output transistor drain, b output	b register	VDDb
29	Output transistor source, b output	b register	OUTb
30	Substrate and Package Ground		SUB
31	Reset transistor drain, b output	b register	RDb
32	Reset transistor gate, b output	b register	RGb
33	Last gate, b output	b register	LGb
34 (35)	Serial phase 3, b register	b register	S3b
35 (34)	Serial phase 2, b register	b register	S2b
36	Serial phase 1, common ab register	ab register	S1ab
37 (38)	Serial phase 2, a register	a register	S2a
38 (37)	Serial phase 3, a register	a register	S3a
39	Last gate, a output	a register	LGa
40	Reset transistor gate, a output	a register	RGa
41	Reset transistor drain, a output	a register	RDa
42	Substrate and Package Ground		SUB
43	Output transistor source, a output	a register	OUTa
44	Output transistor drain, a output	a register	VDDa
45	Output Ground Reference	a register	GNDa
46	Summing well, a output	a register	SWa
47	Transfer gate, upper serial register	ab register	TGa
48	Parallel phase 1	upper quadrants	P1a
49	Parallel phase 2	upper quadrants	P2a
50	Parallel phase 3	left common	P3ac
51	Parallel phase 2	lower quadrants	P2c
52	Parallel phase 1	lower quadrants	P1c
53	Transfer gate, lower serial register	cd register	TGc
54	Summing well, c output	c register	SWc
55	Output Ground Reference	c register	GNDc
56	Output transistor drain, c output	c register	VDDc

TABLE 3 *pin definitions*

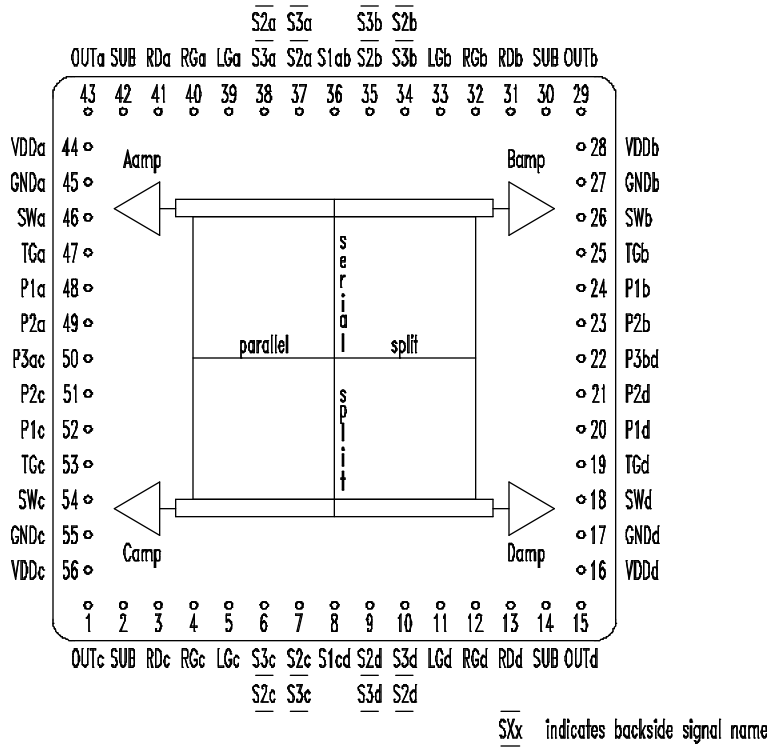

FIGURE 5 SI-003A *pin labels*

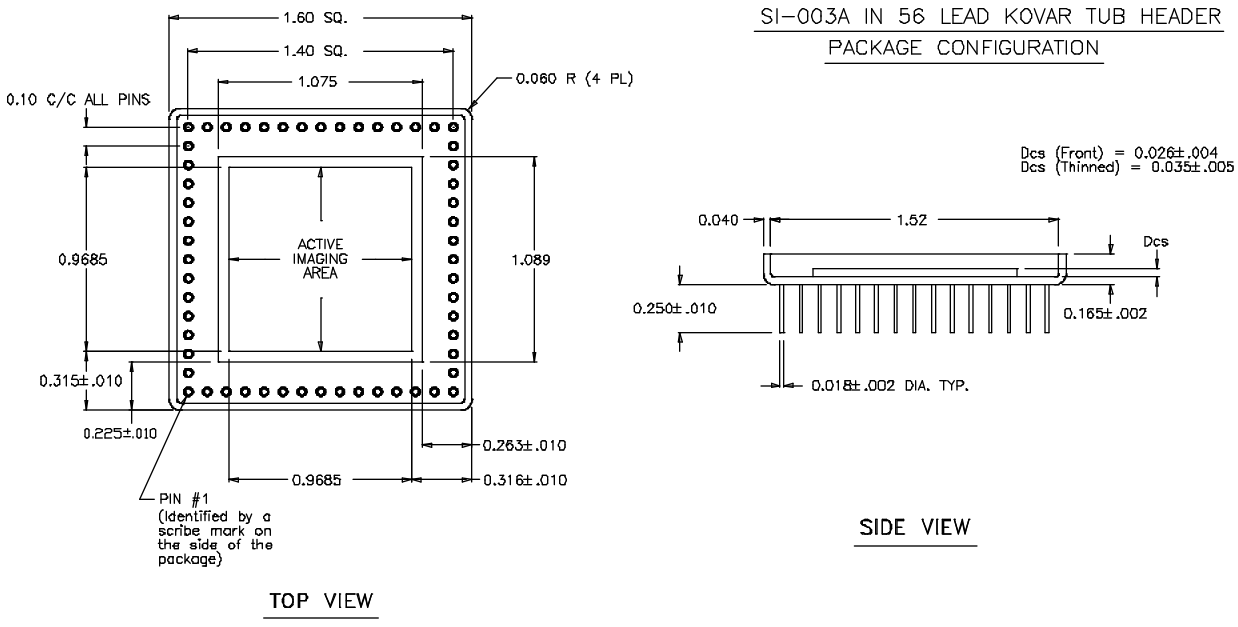

FIGURE 6 SI-003A *package configuration*

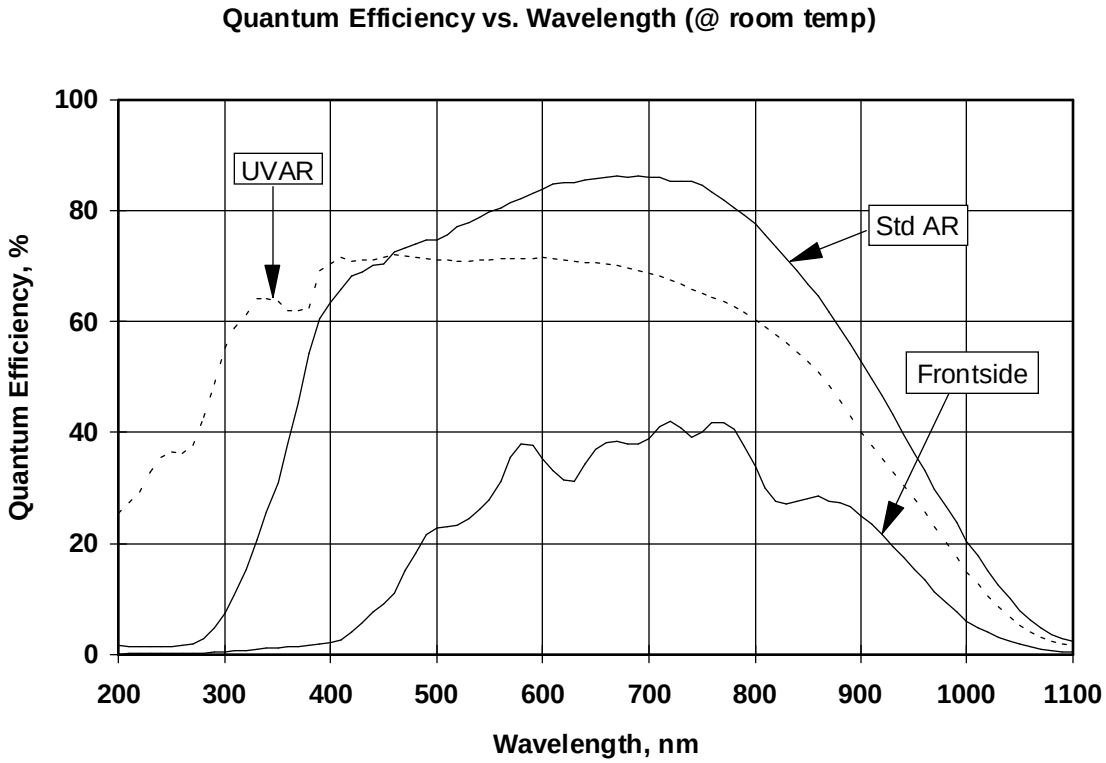

FIGURE 7 *Typical QE curves*

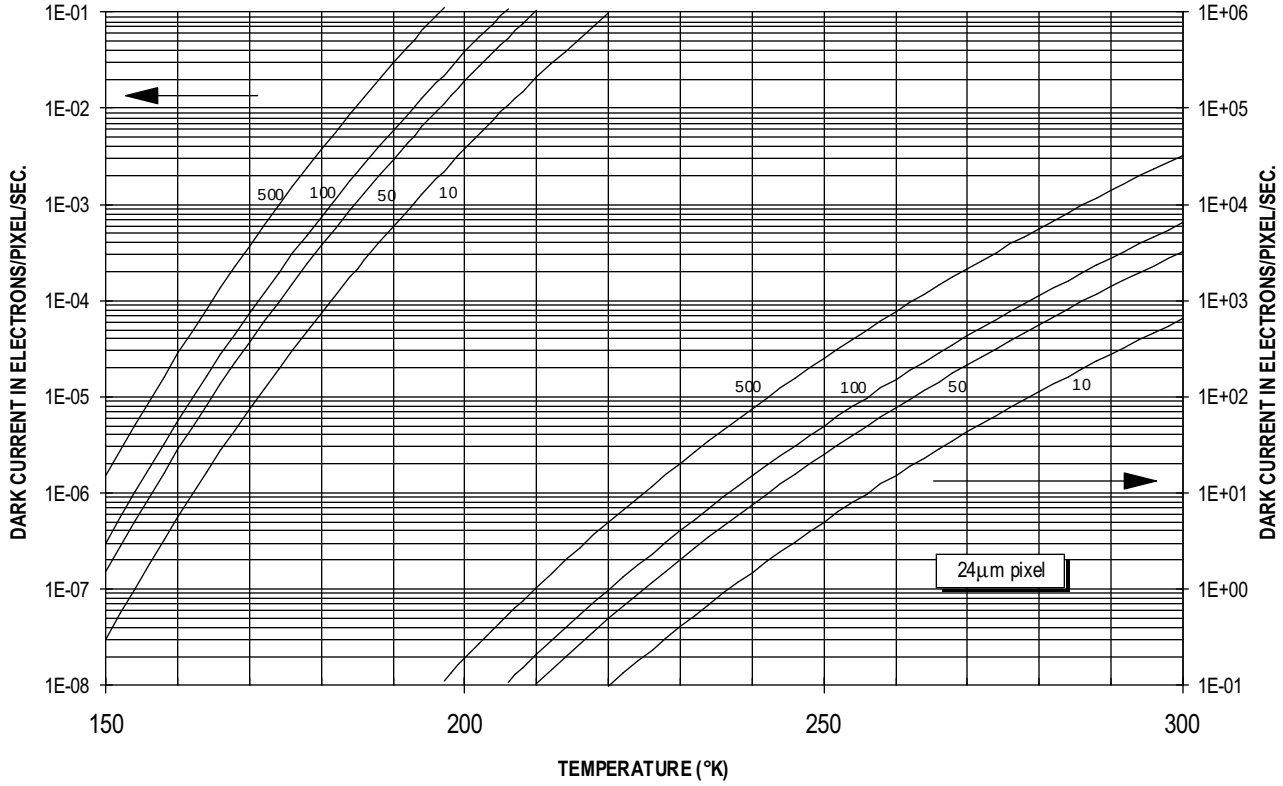

FIGURE 8 *Effect of temperature on dark current. Parameter is pAmp/cm^2 at 293K*

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Scientific Imaging Technologies, Inc. (SITe) specializes in the research, design, and manufacture of charge-coupled devices (CCDs) and imaging subassemblies containing CCD components. SITe's scientific grade CCDs are used in applications for astronomy, aerospace, medical, military surveillance, spectroscopy, and other areas of imaging research. Commercial uses of SITe high performance CCDs include such areas as biomedical imaging, manufacturing quality control, environmental monitoring, and nondestructive testing.

With its focus on scientific-grade CCD imaging components and modules, SITe provides standard designs, user defined custom CCDs, and foundry services. SITe's engineering and manufacturing team builds custom CCD imagers for use in the most demanding applications including NASA programs, satellite platforms, and other research projects. Device formats are available as front illuminated or thinned, back illuminated CCDs.

Innovation, process development, and design experience date back to the founding of the group in 1974.

Product Precautions

Scientific Imaging Technologies, Inc. (SITe) realizes the use of charge-coupled devices (CCDs) for imaging is rapidly expanding into new applications. Awareness of the sensitivity of CCDs to electrostatic discharge (ESD) damage and the steps that can be implemented to prevent damage are very important to the end user.

With the exception of the back-illuminated SI424A, SITe imagers do not have built-in gate protection structures. Even with the protection structures, the imagers are very sensitive to ESD damage. It is imperative that proper precautions be taken whenever the imagers are handled.

The damage caused by ESD can be immediate and fatal (hard damage) resulting in a completely nonfunctional device. ESD damage can also be more subtle with no immediate device performance degradation. In this case, the result is a slow deterioration (soft damage) that may not be apparent until after extended operation.

There are three major areas where special procedures are required. We recommend that our customers use these procedures to minimize the risk of ESD damage.

1. Work areas specifically designed to minimize ESD.

2. Personnel requirements for ESD damage protection.

3. Use special ESD protected handling and shipping containers. SITe has developed a custom shipping container which grounds all the CCD pins together and allows clean and safe handling for incoming inspection and storage.

For more specific information on minimizing ESD damage, refer to SITe's technical briefing called "Recommended ESD Handling Procedures For CCD Imagers."

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